In the Claims:

1-6. cancelled

7. (new) An integrated circuit comprising:

A. functional circuitry having data input leads and data output leads;

B. test access port circuitry having a test data input lead, a test data output lead, a mode select lead, a test clock lead, a scan circuitry control output lead, and a data register connected in series between the test data input lead and the test data output lead, the data register having a serial data output lead and a serial data input lead;

C. scan test port circuitry having a scan input lead connected to the serial data output lead, a scan output lead connected to the serial data input lead, a scan enable input lead, a capture select input lead, a scan clock input lead, and a scan register connected between the scan input lead and the scan output lead, the scan register having functional data output and input leads connected to the functional circuitry data input and output leads; and

D. connection circuitry coupling the scan test port circuitry to the test access port circuitry, the connection circuitry having inputs connected to the scan circuitry control output lead, the test mode input lead, the test clock input lead, and the connection circuitry being connected to the scan enable input lead, the capture select input lead, and the scan clock input lead.

8. (new) The integrated circuit of claim 7 including a gate selectively coupling the scan output lead to the test data output lead.

9. (new) The integrated circuit of claim 8 including a lock out signal lead coupled to the gate selectively to control coupling the scan output lead to the test data output lead.

10. (new) The integrated circuit of claim 7 including a gate selectively connecting a test mode signal to the test mode lead.

11. (new) The integrated circuit of claim 11 including a lock out signal lead coupled to the gate selectively to control coupling the test mode signal to the test mode lead.

12. (new) The integrated circuit of claim 7 in which the test access port circuitry includes an instruction register connected in series between the test data input lead and the test data output lead, the instruction register having an output lead connected to the scan circuitry control output lead.

13. (new) The integrated circuit of claim 7 in which the test access port circuitry includes a TAP controller connected to the mode select lead and the test clock lead, the TAP controller having an output lead connected to an input of the connection circuitry.